REMARKS

Claim 1 has been amended. No claims are added or canceled hereby. Accordingly, after entry of this Amendment, claims 1-3 will remain pending.

In the non-final Office Action dated July 24, 2006, the Examiner rejected claims 1 and 3 under 35 U.S.C. § 103(a) as being unpatentable over Benaissa et al. (U.S. Patent Application Publication No. 2002/0084494) in view of Delgado et al. (U.S. Patent No. 5,959,508) or Chang (U.S. Patent No. 6,069,091). The Applicant respectfully disagrees with this rejection and, therefore, respectfully traverses the same.

In the Office Action, the Examiner indicated that claim 2 was rejected as being dependent upon a rejected base claim. The Examiner also indicated that claim 2 would be considered allowable is rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant would like to thank the Examiner for the indication of allowable subject matter. Given the Amendments presented above and the remarks that follow, the Applicant has elected, at this time, not to amend claim 2 to place the claim in condition for allowance as a separate independent claim.

The Applicant respectfully submits that claims 1-3 are patentable over the art cited by the Examiner because the claims recite a method of forming device isolation structures in an embedded semiconductor device that combine a number of features including, among them, providing a semiconductor substrate having a first area for a power device in which a first type impurity ions are implanted and a second area for a logic device. None of the references relied upon by the Examiner describe or suggest at least these features. Accordingly, the Applicant respectfully submits that the references cannot be relied upon, either alone or in combination, to render any of claims 1-3 obvious.

Benaissa et al. describes a method for making high gain bipolar transistors in a CMOS process. According to the reference, Fig. 1 illustrates a conventional design for an npn bipolar transistor in a CMOS process. (Benaissa et al. at paragraph [0015].) The CMOS devices are separated by shallow trench isolation 102. (Benaissa et al. at paragraph [0015].) A p-well 104 is located beneath the n source/drain 106, with the n-well serving as the emitter. (Benaissa et al. at paragraph [0015].) A deep n-well 108 is located beneath the p-well. (Benaissa et al. at paragraph [0015].)

Fig. 2 illustrates the construction of the device according to Benaissa et al. In Fig. 2, the p-well is replaced with monocrystalline silicon such that the two n-wells and a deep p-well surround an epi layer, which is situated beneath the n source/drain. (Benaissa et al. at paragraph 0016].) Since the new base has a lower carrier concentration relative to the emitter, the emitter efficiency is improved over the convention design illustrated in Fig. 1. (Benaissa et al. at pargraph [0016].)

At no point does Benaissa et al. describe or suggest a semiconductor substrate having a first area for a power device in which a first type impurity ions are implanted and a second area for a logic device. Moreover, there is no discussion in Benaissa et al., as recognized by the Examiner, of forming a first device isolation region through partial oxidation in the first area. While the Examiner asserts that the first area of the substrate is the area where the DEEP NWELL, PWELL and EMITTER are located and that a first device isolation region (labeled 1) is in the first area, the Applicant respectfully submits, among other things, that this characterization appears to be inaccurate. Neither the area (labeled 1 by the Examiner) nor the area (labeled 2 by the Examiner) are discussed by Benaissa et al. Accordingly, there is no information provided by the reference that the Applicant believes justifies the conclusion reached by the Examiner. Among other things, there is not discussion of implanting first type impurity ions in the first area identified by the Examiner. Moreover, there is no discussion of forming a first isolation region through partial oxidation of the first area. Accordingly, the reference cannot be relied upon as a primary reference on which to base a rejection of claims 1-3 under 35 U.S.C. § 103(a).

The Applicant also respectfully submits that the remaining two references relied upon by the Examiner do not assist with a rejection of claims 1-3 because these two references do not cure the deficiencies noted with respect to Benaissa et al. While Delgado et al. describes defect guttering by induced stress, there is nothing in the reference that suggests the reference may be combined with Benaissa et al. to arrive at the combination recited by claims 1-3. Chang et al. is similarly deficient.

Each of the rejections having been addressed, the Applicant respectfully requests that the Examiner reconsider the rejection of the claims, withdraw the rejection, and pass this application quickly to issuance.